IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A method of transferring a data stream comprising:

directly transferring a plurality of bits associated with a data stream from an external data source device to a temporary storage associated with a different device, wherein each device includes its own storage and processing capabilities, and wherein the temporary storage is equipped to concurrently handle multiple additional data streams with the data stream;

concurrently intercepting during the transfer each bit associated with the data stream and counting a bit-transfer total and a bit-set total associated with the data stream; and

determining if the bit-set total exceeds more than half the bit-transfer total and if so setting an inversion flag bit which is associated with the data stream, and wherein the processing of the method and the temporary storage reside within a same controller as one another, and wherein the inversion flag for the data stream is set but the data stream remains unchanged until and when the data stream is transferred out of the temporary storage, and wherein the inversion flag bit is part of [[a]] bytes ~~separate data stream~~ maintained within the temporary storage, each bit ~~of the separate date stream~~ representing a ~~different inversion flag bit for different~~ single unique data stream [[streams]] and at least one bit representing the inversion flag bit for the data stream~~, a position of each bit within the separate data stream identifying a particular data stream to which it relates~~.

2. (Original) The method of claim 1, further comprising:

transferring from the temporary storage to a target source each bit associated with the data stream and concurrently inverting each bit as transferred, if the inversion flag bit is set.

3.- 6. (Canceled)

7. (Currently Amended) A method of transferring a data stream, comprising:

directly receiving a data stream and an inversion flag associated with the data stream from an external data source device into a different device, wherein each device includes its own storage and processing capabilities, and wherein the data stream remains unchanged in the external data source even when an inversion flag has been set for the data stream in the external data source, and wherein the inversion flag is part of bytes housed in a register ~~a different data stream~~ where each bit ~~of the different data stream~~ identifies a single unique ~~particular~~ data stream ~~and that particular data stream's inversion flag~~;

transferring one or more bits associated with the data stream from the external data source device to a target source, if the inversion flag is unset; and

inverting the bits associated with the data stream as the data stream is transferred from the external data source device to the target source, if the inversion flag is set, wherein the data stream is processed and temporarily housed in storage within a same controller as it is transferred to the target source, and wherein the storage is equipped to concurrently house and process additional data streams with the data stream.

8.-10. (Canceled)

11. (Currently Amended) A computer readable medium having executable instructions for executing a method which is operable to invert transferred data, the method comprising:

acquiring a data stream and an inversion flag directly from an external data source device;

separating the data stream and the inversion flag into a data stream storage and an inversion flag storage; and

buffering one or more additional data streams and one or more additional inversion flags from the data source device in the storages, within a same controller associated with a different device than the data source device, and wherein each device includes its own storage and processing capabilities, and wherein the data stream storage concurrently houses and processes additional data streams with the data stream, and wherein the data stream with a set inversion flag remains unchanged until requested at which time the data stream is inverted as it is

transferred out, and wherein the inversion flag storage includes bytes ~~a different data stream~~ where each bit ~~of the different data stream~~ corresponds to a single unique ~~particular inversion flag for a particular~~ data stream

12. (Original) The medium of claim 11, further comprising:

inverting all bits associated with a transferred data stream as the transferred data stream is sent to a target source from the data stream storage, if a corresponding inversion flag associated with the transferred data stream is set in the inversion flag storage.

13.-16. (Canceled)

17. (Currently Amended) An inversion data transfer system, comprising:

an external data source device;

a temporary storage associated with a different device from that of the external data source device; and

a controller that directly transfers a data stream having a plurality of bits from the data source device to the temporary storage, and concurrent to the transfer determines if a total number of set bits within the data stream is more than half of a total number of bits associated with the data stream, and if so associating a set inversion bit with the data stream, otherwise associating an unset inversion bit with the data stream, wherein the temporary storage resides within the controller and on the same device as the temporary storage and separate from the external data source device, and wherein each device includes its own storage and processing capabilities, and wherein the temporary storage is to concurrently handle and process additional data streams with the data stream, and wherein the data stream remains unchanged in the temporary storage when the inversion bit is set until and when it is transferred out of the temporary storage at which time it is inverted, and wherein the inversion bit is part of bytes ~~a different data stream~~ managed by the controller where each particular bit ~~of the different data stream~~ represents a single unique ~~particular inversion bit for a particular~~ data stream.

18. (Original) The system of elaim 17, further comprising:

a target souree device whieh conеurrently receives the bits of the data stream inverted, as the data stream is transferred from the temporary storage, if a set inversion bit associated with the data stream is detected.

19. (Canceled)

20. (Original) The system of claim 19, wherein the controller further retrieves from the register storage each inversion bit associated with a transferred data stream and is operable to concurrently transfer the transferred data stream from the temporary storage and invert the bits associated with the transferred data stream if the inversion bit is set.

21. (Currently Amended) An inversion data transfer system, comprising:

an external data source device;

a target source device, wherein the external data source device and the target souree device are different from one another and two separate devices, and wherein each device includes its own storage and processing capabilities; and

a controller that directly acquires a data stream and an inversion bit associated with the data stream from the data source device and inverts bits associated with the data stream during a transfer of the data stream to a target source device, if the inversion bit is set, and wherein the controller buffers the data stream before it is transferred to the target souree device within the controller, and wherein the controller uses a buffer to buffer the data stream eoncurrently with additional data streams, and wherein the data stream remains unchanged within the data source device and is inverted when the inversion bit is set and when transferred out of the data souree device to the target source device, and wherein the inversion bit is associated with bytes ~~a different data stream~~ where each bit ~~of the different data stream~~ corresponds to a single unique ~~particular inversion bit for a~~ particular data stream.

22. (Original) The system of claim 21 further comprising:

a temporary storage operable to house the data stream as the data stream is acquired from the data source device; and

a register storage operable to house the inversion bit as the data stream is acquired from the data source device.

23.-24. (Canceled)

25. (Currently Amended) A system for transferring a data stream, comprising:

a control buffer;

a storage buffer;

an inversion storage;

a counting set of executable instructions to count set bits associated with a data stream being received from the control buffer directly into the storage buffer, wherein the control buffer is an external data source to the storage buffer, and the counting set of executable instructions generates an inversion bit associated with the data stream, wherein the inversion bit is housed in the inversion storage and is set if a total number of set bits exceeds more than half a total number of bits associated with the data stream, and wherein the inversion storage, the storage buffer, and the counting set of instructions reside within a same controller and device that is different from another device associated with the control buffer that supplies the data stream, and wherein each device includes its own storage and processing capabilities, and wherein the storage buffer is to concurrently handle and process additional data streams with the data stream, and wherein the data stream remains unchanged in the storage buffer and is inverted when it is transferred out of the storage buffer when the inversion bit is set in the inversion storage, and wherein [[a]] bytes ~~different data stream is~~ are maintained in the inversion storage that includes the inversion bit and where each bit ~~of the different data stream~~ corresponds to a single unique ~~particular inversion bit for a particular~~ data stream.

26. (Original) The system of claim 25, further comprising:

a transfer set of executable instructions operable to use the counting set of executable instructions to transfer the data stream from the storage buffer to a target device, wherein the entire data stream is inverted if the inversion bit is set as the data stream is being transferred to the target device.

27. (Original) The system of claim 26, wherein the inversion bit is transferred with the data stream to the target device.

28.-32. (Canceled)

33. (Currently Amended) A memory apparatus, comprising:

an inversion bit;

a data packet;

a state machine that controls the transfer of the data packet to a target device wherein the packet is inverted as it is transferred to the target device, if the inversion bit is set, and wherein the state machine directly receives the data packet from an external data source device and processes the data packet within the apparatus, wherein the data packet remains unchanged within the external data source and is inverted when transferred out of the external data source when the inversion bit is set, and wherein the external data source device is separate from a device representing the apparatus, and wherein each device includes its own storage and processing capabilities, and wherein temporary storage is used for buffering the data packet of a data stream and the temporary storage is also used to concurrently handle other data packets associated with other data streams, and wherein the inversion bit is part of bytes ~~a different data stream~~, where each bit ~~of the different data stream~~ corresponding to a single unique ~~particular inversion bit associated with a particular~~ data stream.

34. (Original) The apparatus of claim 33, further comprising:

a buffer to house the data packet prior to transfer to the target device; and

a register to house the inversion bit.

35. (Original) The apparatus of claim 33, wherein the state machine is configured by interfacing one or more electro-mechanical devices.

36. (Original) The apparatus of claim 33, wherein the state machine is configured using a set of executable instructions.

37. (Original) The apparatus of claim 33, wherein the data packet is a fixed length data packet.

38. (Original) The apparatus of claim 33, wherein the data packet is a variable length data packet.

39. (Original) The apparatus of claim 33, wherein the apparatus is a flash memory device.

40. (Currently Amended) A flash memory device, comprising:

a temporary storage;

a receiving controller;

a counting controller; and

a transferring controller that transfers a data packet directly received by the receiving controller in a temporary storage to an external target device and further inverts the data packet during the transfer if the counting controller indicates to the transferring controller that the packet requires inversion, wherein the data packet remains unchanged in the temporary storage and is inverted while it is transferred out of the temporary storage when the controller indicates to do so, and wherein the counting controller and the temporary storage reside within the transferring controller device, and wherein each device includes its own storage and processing capabilities, and wherein the temporary storage is concurrently used to house and process other data packets associated with other data streams with the data packet, and wherein an inversion bit is associated with the data packet to indicate to the transferring controller whether the data packet required inversion and a two-byte word ~~a different data stream~~ includes the inversion bit

and each bit of the two-byte word ~~different data stream~~ corresponds to single unique ~~an inversion bit for a particular data packet or~~ data stream.

41. (Original) The flash memory device of claim 40, wherein the counting controller indicates the packet requires inversion if a total number of set bits associated with the packet exceeds more than half a total number of bits associated with the packet.

42. (Original) The flash memory device of claim 40, wherein the memory device is at least one of a compact flash memory card and a multimedia card.

43. (Original) The flash memory device of claim 40, wherein the memory device is included in the operation of a at least one of a digital camera device, digital video device, and a portable audio player device.

44.-46. (Canceled)